A Grid Connected Single Phase Transformerless Inverter Controlling Two Solar PV Arrays Operating under Different Atmospheric Conditions

Subhendu Dutta, Dipankar Debnath, *Member*, *IEEE*, and Kishore Chatterjee, *Member*, *IEEE*

***Abstract*—A grid connected single phase transformerless inverter which can operate two serially connected solar photo voltaic (PV) subarrays at their respective maximum power points while each one of them is exposed to different atmospheric conditions is proposed in this paper. As two subarrays are connected in series, the number of serially connected modules within a subarray is reduced to half. Reduction in the number of serially connected PV modules within a subarray leads to an overall improvement in the magnitude of power that can be abstracted from a subarray while the modules of the subarray are exposed to varied atmospheric conditions. The topological structure of the inverter ensures that the common mode voltage does not contain high frequency components, thereby reducing the magnitude of leakage current involved with the solar panels well within the acceptable limit. An in depth analysis of the scheme along with the derivation of its small signal model has been carried out. Detailed simulation studies are performed to verify its effectiveness. A 1 kW laboratory prototype of the scheme has been fabricated. Detailed experimental validations have been carried out utilizing the prototype to confirm the viability of the proposed scheme.**

***Index Terms*—Grid connected single phase transformerless PV inverter, Maximum power extraction, Mismatched operating condition, Serially connected PV subarrays.**

I. Introduction

SINGLE phase Transformerless Grid Connected Systems (TLGCS) have become popular over the years due to its reduced size, weight, volume and increased operating efficiency [1], [2]. However, in TLGCS the dc link voltage of the inverter needs to be high. As a result the number of modules that needs to be connected in series becomes large. When large number of modules are connected in series, power yield from the array gets substantially reduced when the modules are subjected to varied environmental conditions such as shading [3]- [5]. The topologies derived from H-bridge based inverter [6]- [12] and the topologies presented in [13], [14] which use single photo voltaic (PV) source as their input are prone to this mismatched operating problem more because number of series connected modules are more. The topologies derived from neutral point clamped (NPC) based inverter [15]- [19] are severely affected by mismatched operating problem as they require double the magnitude of PV voltage compared to conventional H-bridge based inverter topologies.

In order to overcome the aforementioned problem attempts have been made to abstract maximum available power from each of the PV modules while they are exposed to mismatched operating conditions. Schemes based on Generation Control Circuit [4], [5] attempt to achieve it by redistributing the power obtained from subarrays among themselves so that all the subarrays are operated at their respective maximum power point (MPP)s. However, they are realized by having two stage configuration and thereby have a complex control algorithm, and their operating efficiency is low. Further, the efficiency of these schemes are highly dependent on the level of shading to which each of the subarrays are exposed. Schemes based on module integrated converters (MIC) and multi-input string inverters are also reported in the literature which also attempt to control each and every PV module present in the array [2]. However, they require the involvement of an additional dc to dc converter stage prior to the dc to ac inverter stage. This additional stage involving several dc to dc converters increases the component count thereby reducing efficiency and reliability of the system [20], [21].

The aforementioned problems associated with MIC and multi-input string inverters are overcome in switched PV based system [22] and voltage injection based system [23] at the cost of increasing the active component count leading to the decrement in efficiency and reliability of the overall system. Further, in case of voltage injection based schemes the shaded modules are bypassed. Hence to achieve sufficient DC bus voltage during shaded condition, number of modules to be included in a subarray needs to be more compared to that of the other schemes thereby increasing the cost of the system.

In order to reduce the number of components and to simplify the control complexity, attempts have been made to form a subarray with desired number of PV modules connected in series as per the input voltage requirement of the particular system. Two such subarrays so formed are then connected in series and each of these subarrays is being controlled to operate at their respective MPPs [20], [24]- [28]. By segregating the modules in two subarrays and subsequently operating the two serially connected subarrays at their respective MPPs, the yield of power during non uniform environmental condition is enhanced without increasing the number of power processing stages. However, the schemes presented in [24], [25] require similar operating condition for the two PV subarrays to limit the magnitude of DC current injection into the grid within permissible range [29]. Schemes involving T-type power circuit configuration are reported for three phase [26], [27] as well as single phase [29], [30] applications. T-type based single phase half bridge configurations [29], [30] require double the number

of serially connected PV modules in a subarray as compared to full bridge configuration thereby making the efficacy of the scheme ineffective during mismatched operating conditions. Further, single phase full bridge T-type configuration poses a serious limitation while operating under mismatched operating conditions. This is due to the fact that while in operation under mismatched condition, the duty ratios of the pertinent high frequency switches which are in operation during positive half cycle become different from each other. And the same is true for the pertinent high frequency switches which are in operation during negative half cycle. The asymmetry in duty ratios of the switches causes considerable variation in the common mode voltage thereby increasing the magnitude of the leakage current beyond the prescribed limit. Due to this issue such a scheme has not been reported in the literature for PV application. T-type three phase solar PV based grid connected systems are also reported in the literature [26], [27] however, they are generally employed when the power level becomes more than 10 kW. Hence they cannot be considered for single phase grid connected application where power level is around 5 kW [20]. The scheme presented in [20] involves two stages of power processing and the overall improvement in efficiency of the system depends on the extent of mismatch that exists between the two subarrays. Although the scheme presented in [28] utilizes single stage of power processing, the overall efficiency of the system is poor as the buck-boost based dc to ac inverter is designed to operate in discontinuous mode of conduction (DCM).

In this paper a new inverter topology which is derived by combining two half bridge inverters along with their respective ac bypass is proposed wherein two serially connected subarrays are controlled individually by these two half bridge inverters. The required voltage level at MPP (V_{mpp}) for each of the subarrays in case of the proposed topology is required to be 200 V while V_{mpp} requirement for each of the subarrays in [20] is 400 V. Hence the number of serially connected modules required in each of the subarrays of the proposed scheme is half to that of [20], and therefore the power yield from the proposed scheme is better compared to that of [20] while operating under mismatched operating condition. Although the scheme proposed in [28] requires V_{mpp} for each of the solar subarrays to be 200 V, the overall efficiency of the scheme is poor as it is based on buck-boost based topology operating under DCM. The European efficiency (η_{euro}) of the scheme proposed in this paper is found to be 96% which is higher than that of [20] and [28] when all the subarrays are being operated under uniform environmental condition. When the subarrays are being operated under mismatched environmental condition, the measured efficiency of the proposed scheme is found to be even higher than that of [20] and [28]. Further, the magnitude of the leakage current in the proposed scheme is maintained within the specified limit while having all the other advantages that would have been there in case of a T-type full bridge based transformerless single phase solar PV system.

The operating principle of the proposed scheme is explained in detail in Section II by exploring all the equivalent topological stages. Subsequently the mathematical analysis of the scheme has been carried out and the small signal model of the scheme has been derived in Section III. The philosophy of control is described in detail and the configuration of the controller is derived in Section IV. The design guidelines for selecting the filter components of the inverter are presented in Section V. Detailed simulation studies are carried out to verify the performance of the scheme in Section VI. A laboratory prototype of the scheme having a power rating of 1 kW has been fabricated. Exhaustive experimental studies are carried out utilizing the laboratory prototype to confirm the viability of the scheme and presented in Section VII.

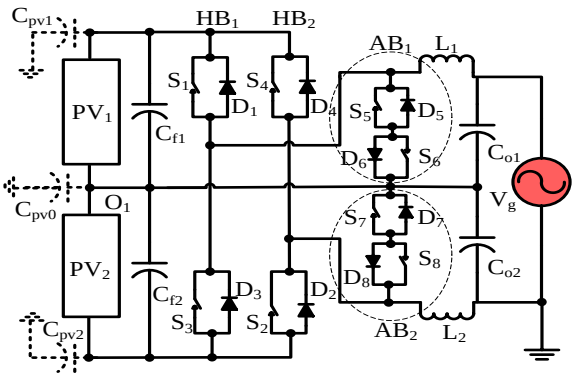

Fig. 1. Combined Half Bridge Inverter with AC Bypass (CHBIAB)

II. Operating Principle of the Proposed Inverter

The schematic circuit diagram of the Combined Half Bridge Inverter with AC Bypass (CHBIAB) which is proposed in this paper is shown in Fig. 1. Half bridge (HB_1) of one of the component inverters ($HBIAB_1$) is formed by the switches, S_1, D_1 and S_3, D_3 while its AC bypass (AB_1) is constituted by S_5, D_5 and S_6, D_6. L_1, C_{o1} serve as its output filter components. The half bridge (HB_2) of another component inverter ($HBIAB_2$) is formed by S_2, D_2 and S_4, D_4 while its AC bypass (AB_2) is constituted by S_7, D_7 and S_8, D_8. L_2, C_{o2} serve as its output filter components. The input side filter capacitors are C_{f1} and C_{f2} while PV array to ground parasitic capacitors are considered to be C_{pv0}, C_{pv1} and C_{pv2}. PV_1 and PV_2 represent two subarrays under consideration.

In order to ensure that the current fed by the inverter to the grid is sinusoidal, duty ratio of the switches, S_1 and S_2 are varied sinusoidally during positive half cycle (PHC). Further, the sinusoidal switching pulse train is synchronized with the grid voltage (v_g) to ascertain unity power factor operation. In the negative half cycle (NHC) the switches S_3 and S_4 are operated in similar way the switches, S_1 and S_2 are operated in PHC. During PHC, the switches, S_6 and S_8 are permanently kept on while switches, S_3, S_4, S_5 and S_7 are permanently kept off, whereas during NHC the switches, S_5 and S_7 are permanently kept on while switches, S_1, S_2, S_6 and S_8 are permanently kept off. The path for power flow during active state in PHC (when S_1 and S_2 are on) is shown in Fig. 2(a) while Fig. 2(b) shows the condition of the freewheeling state during PHC (when S_1 and S_2 are off). In NHC power flow path during active state (when S_3 and S_4 are on) is shown in

Fig. 2(c) while Fig. 2(d) shows the freewheeling state in NHC (when S_3 and S_4 are off).

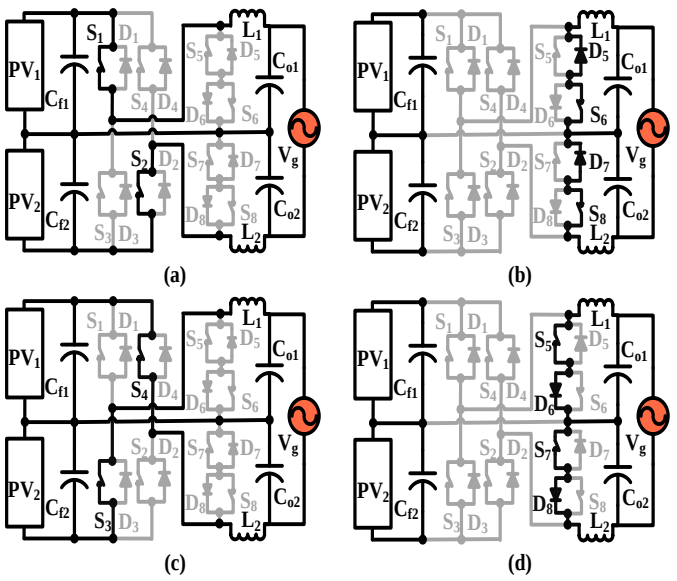

Fig. 2. Topological stages of the proposed inverter: (a) Active stage of PHC, (b) Freewheeling stage of PHC, (c) Active stage of NHC, (d) Freewheeling stage of NHC

In order to analyze the operation of the CHBIAB, simplified block diagrams representing its operation in PHC and NHC are depicted in Fig. 3(a) and Fig. 3(b) respectively. Depending on the variation in insolation level, temperature and other atmospheric conditions, P_{mpp1}, V_{mpp1}, I_{mpp1} pertaining to the subarray, PV_1 differs from P_{mpp2}, V_{mpp2}, I_{mpp2} pertaining to the subarray, PV_2 wherein P_{mpp1} is the maximum power (P_{mpp}) that can be abstracted from PV_1 while V_{mpp1} and I_{mpp1} are the corresponding subarray voltage (V_{mpp}) and current (I_{mpp}) at MPP. Similarly P_{mpp2} is the maximum power that can be abstracted from PV_2 while V_{mpp2} and I_{mpp2} are the corresponding subarray voltage and current at MPP. The power abstracted from PV_1 and PV_2 are dumped on to C_{o1} and C_{o2} respectively during PHC while during NHC the power abstracted from PV_1 and PV_2 are dumped on to C_{o2} and C_{o1} respectively. Hence during PHC

$$P_{gco1} = P_{mpp1} \quad \& \quad P_{gco2} = P_{mpp2} \tag{1}$$

while during NHC

$$P_{gco1} = P_{mpp2} \quad \& \quad P_{gco2} = P_{mpp1} \tag{2}$$

wherein P_{gco1} and P_{gco2} are powers averaged over a half cycle and associated with C_{o1} and C_{o2} respectively. The average power fed to the grid at steady state, P_g can be expressed as

$$P_g = P_{mpp1} + P_{mpp2} \tag{3}$$

Further,

$$v_g = v_{co1} + v_{co2} \tag{4}$$

wherein v_g is the instantaneous grid voltage while v_{co1} and v_{co2} are the instantaneous voltages across C_{o1} and C_{o2} respectively. v_{co} represents both v_{co1} and v_{co2}. The instantaneous power fed to the grid, p_g can be expressed as

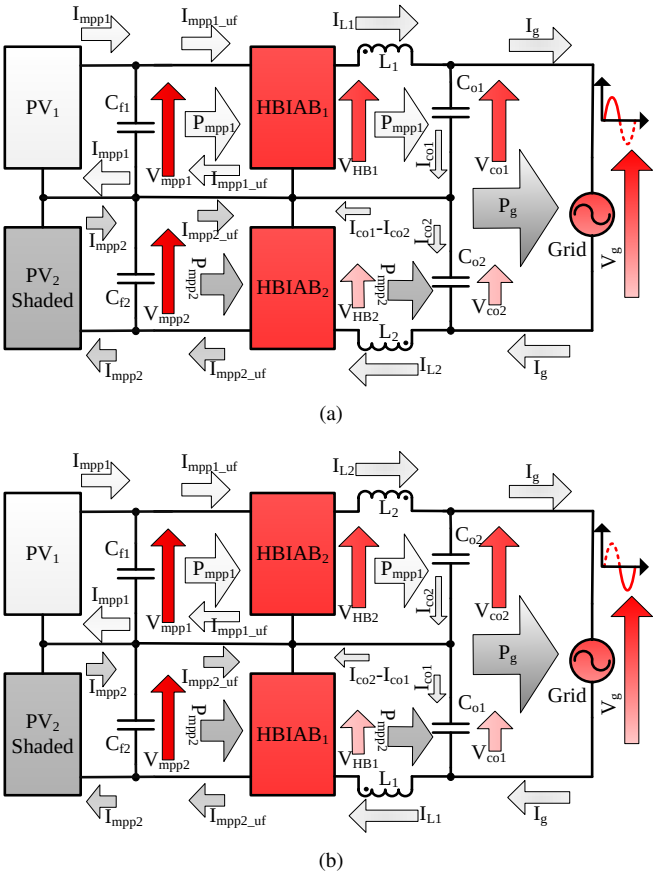

Fig. 3. Power flow block diagram during (a) PHC, (b) NHC

$$p_g = v_g i_g = (v_{co1} + v_{co2}) i_g \tag{5}$$

wherein i_g is the instantaneous grid current. As the inverter is made to feed power to the grid at unity power factor,

$$I_g = \frac{P_g}{V_g} \tag{6}$$

wherein V_g and I_g are the rms grid voltage and current respectively.

1) Operation during PHC: It can be noted that the power fed to the grid averaged over PHC remains the same as the power, P_g fed to the grid averaged over the full cycle. Hence,

$$\begin{aligned} P_g &= \frac{1}{\pi}\int_0^{\pi} p_g \, d(\omega t) \\ &= \frac{1}{\pi}\int_0^{\pi} v_{co1} i_g \, d(\omega t) + \frac{1}{\pi}\int_0^{\pi} v_{co2} i_g \, d(\omega t) \quad (7) \\ &= P_{gco1} + P_{gco2} \quad (8) \end{aligned}$$

It can be inferred from (4) that v_{co1} and v_{co2} are having the same frequency and phase as that of v_g. Hence

$$P_{gco1} = \frac{1}{\pi}\int_0^{\pi} V_{co1m} sin(\omega t) I_{gm} sin(\omega t) \, d(\omega t) = \frac{V_{co1m} I_{gm}}{2} \tag{9}$$

$$P_{gco2} = \frac{1}{\pi}\int_0^{\pi} V_{co2m} sin(\omega t) I_{gm} sin(\omega t) \, d(\omega t) = \frac{V_{co2m} I_{gm}}{2} \tag{10}$$

wherein V_{co1m}, V_{co2m} and I_{gm} are amplitudes of v_{co1}, v_{co2} and i_g respectively. Again, V_{com} represents both V_{co1m} and V_{co2m}. Combining (1), (9) and (10)

$$V_{co1m} = \frac{2P_{mpp1}}{I_{gm}} = \frac{\sqrt{2}P_{mpp1}}{I_g} = \frac{\sqrt{2}P_{mpp1}}{P_g/V_g} \tag{11}$$

$$V_{co2m} = \frac{2P_{mpp2}}{I_{gm}} = \frac{\sqrt{2}P_{mpp2}}{I_g} = \frac{\sqrt{2}P_{mpp2}}{P_g/V_g} \tag{12}$$

Combining (3), (11) and (12),

$$V_{co1m} = \frac{\sqrt{2}V_g P_{mpp1}}{P_{mpp1} + P_{mpp2}} \tag{13}$$

$$V_{co2m} = \frac{\sqrt{2}V_g P_{mpp2}}{P_{mpp1} + P_{mpp2}} \tag{14}$$

2) Operation during NHC: Following the steps similar to that of PHC, the expression for V_{co1m} and V_{co2m} during NHC can be derived as

$$V_{co1m} = \frac{\sqrt{2}V_g P_{mpp2}}{P_{mpp1} + P_{mpp2}} \tag{15}$$

$$V_{co2m} = \frac{\sqrt{2}V_g P_{mpp1}}{P_{mpp1} + P_{mpp2}} \tag{16}$$

The voltages, v_{co1} and v_{co2} varies sinusoidally with amplitudes of V_{co1m} and V_{co2m} respectively. From (13), (14), (15), and (16) it can be inferred that the magnitudes of V_{co1m} and V_{co2m} are dictated by the power evacuated from the PV subarrays. Further, if the power evacuated from PV_1 is greater than PV_2, during PHC $V_{co1m} > V_{co2m}$ while during NHC $V_{co1m} < V_{co2m}$. During PHC the duty ratios, d_1 of S_1 and d_2 of S_2 vary sinusoidally with amplitude d_{1m} and d_{2m} respectively wherein

$$d_{1m} = \frac{V_{co1m}}{V_{mpp1}} \quad \& \quad d_{2m} = \frac{V_{co2m}}{V_{mpp2}} \tag{17}$$

while during NHC the duty ratios, d_3 of S_3 and d_4 of S_4 vary sinusoidally with amplitude d_{3m} and d_{4m} respectively wherein

$$d_{3m} = \frac{V_{co1m}}{V_{mpp2}} \quad \& \quad d_{4m} = \frac{V_{co2m}}{V_{mpp1}} \tag{18}$$

As the output terminals of $HBIAB_1$ and $HBIAB_2$ are connected in series, it can be assumed $i_{L1} = i_{L2} = i_g$ by neglecting currents i_{co1}, i_{co2} flowing through C_{o1}, C_{o2}. Considering switching cycle average of relevant quantities during PHC,

$$\langle i_{mpp1\_uf} \rangle_{T_s} = \langle d_1 \rangle_{T_s} \langle i_g \rangle_{T_s} \,\&\, \langle i_{mpp2\_uf} \rangle_{T_s} = \langle d_2 \rangle_{T_s} \langle i_g \rangle_{T_s} \tag{19}$$

whereas during NHC

$$\langle i_{mpp1\_uf} \rangle_{T_s} = \langle d_4 \rangle_{T_s} \langle i_g \rangle_{T_s} \,\&\, \langle i_{mpp2\_uf} \rangle_{T_s} = \langle d_3 \rangle_{T_s} \langle i_g \rangle_{T_s} \tag{20}$$

wherein i_{mpp1_uf} and i_{mpp2_uf} are the unfiltered currents at the input from PV_1 side and PV_2 side respectively. If the insolation level of PV_1 is higher than that of PV_2 as per (13), (14) and (17), during PHC $d_{1m} > d_{2m}$, thereby $\langle d_1 \rangle_{T_s} > \langle d_2 \rangle_{T_s}$ whereas during NHC as per (15), (16) and (18) $d_{4m} > d_{3m}$, thereby $\langle d_4 \rangle_{T_s} > \langle d_3 \rangle_{T_s}$. Therefore it can be inferred from (19) and (20) that in any half cycle $\langle i_{mpp1\_uf} \rangle_{T_s} > \langle i_{mpp2\_uf} \rangle_{T_s}$, hence $I_{mpp1} > I_{mpp2}$. While the reverse i.e $I_{mpp2} > I_{mpp1}$ is true in any half cycle if the insolation level of PV_2 is higher than that of PV_1.

From the power circuit configuration of the proposed inverter as shown in Fig. 1 it can be noted that the potential of the point, O_1 with respect to earth which is the voltage, v_{cpv0} is equal to v_{co2}. During the operation of the system under unequal atmospheric condition, v_{co2} will have the following components: i) dc component and ii) grid frequency component. The voltage impressed across the parasitic capacitors (v_{cpv}), C_{pv1} and C_{pv2} are v_{cpv1} and v_{cpv2} respectively. And it can be noted that $v_{cpv1} = v_{co2} + V_{mpp1}$ while $v_{cpv2} = v_{co2} - V_{mpp2}$. Hence all the parasitic capacitors, C_{pv0}, C_{pv1} and C_{pv2} are impressed with only low frequency voltage components thereby ensuring that the magnitude of leakage current is low and it is shown in Section VII that for the proposed scheme it remains within the standard permissible limit [29].

III. Mathematical Model of the Scheme

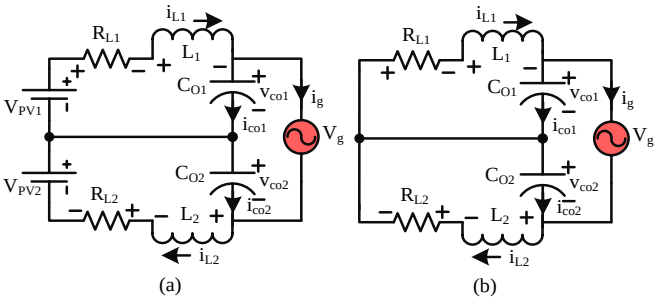

Fig. 4. Equivalent circuit during PHC (a) S_1, S_2 are ON (b) S_1, S_2 are OFF

The small signal model of the proposed inverter is derived by considering the equivalent circuits, Fig. 4(a), 4(b) of the scheme while it is operating in PHC. Parasitic resistances of L_1 and L_2 (R_{L1} and R_{L2}) are considered but equivalent series resistance of C_{o1} and C_{o2} are neglected for simplicity. As i_g is being controlled by manipulating i_{L1}, i_{L2} and v_{co1}, v_{co2}, therefore $i_{L1}(t)$, $i_{L2}(t)$, $v_{co1}(t)$, $v_{co2}(t)$ are considered to be the state variables. The state equations derived from equivalent circuits shown in Fig. 4(a), 4(b) for $HBIAB_1$ are

$$\frac{d}{dt}\begin{bmatrix} i_{L1}(t) \\ v_{co1}(t) \end{bmatrix} = \begin{bmatrix} -\frac{R_{L1}}{L_1} & -\frac{1}{L_1} \\ \frac{1}{C_{o1}} & 0 \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ v_{co1}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} & 0 \\ 0 & -\frac{1}{Z_g C_{o1}} \end{bmatrix} \begin{bmatrix} v_{pv1}(t) \\ v_g(t) \end{bmatrix} \tag{21}$$

$$\frac{d}{dt}\begin{bmatrix} i_{L1}(t) \\ v_{co1}(t) \end{bmatrix} = \begin{bmatrix} -\frac{R_{L1}}{L_1} & -\frac{1}{L_1} \\ \frac{1}{C_{o1}} & 0 \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ v_{co1}(t) \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{Z_g C_{o1}} \end{bmatrix} \begin{bmatrix} v_{pv1}(t) \\ v_g(t) \end{bmatrix} \tag{22}$$

and for $HBIAB_2$

$$\frac{d}{dt}\begin{bmatrix} i_{L2}(t) \\ v_{co2}(t) \end{bmatrix} = \begin{bmatrix} -\frac{R_{L2}}{L_2} & -\frac{1}{L_2} \\ \frac{1}{C_{o2}} & 0 \end{bmatrix} \begin{bmatrix} i_{L2}(t) \\ v_{co2}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_2} & 0 \\ 0 & -\frac{1}{Z_g C_{o2}} \end{bmatrix} \begin{bmatrix} v_{pv2}(t) \\ v_g(t) \end{bmatrix} \quad (23)$$

$$\frac{d}{dt}\begin{bmatrix} i_{L2}(t) \\ v_{co2}(t) \end{bmatrix} = \begin{bmatrix} -\frac{R_{L2}}{L_2} & -\frac{1}{L_2} \\ \frac{1}{C_{o2}} & 0 \end{bmatrix} \begin{bmatrix} i_{L2}(t) \\ v_{co2}(t) \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{Z_g C_{o2}} \end{bmatrix} \begin{bmatrix} v_{pv2}(t) \\ v_g(t) \end{bmatrix} \quad (24)$$

where Z_g is the short circuit impedance of the grid so that $i_g(t) = Z_g v_g(t)$. V_{pv1} and V_{pv2} are the sensed voltage of PV_1 and PV_2 respectively. As the switching frequency is very high compared to the grid frequency, state space averaging based analysis has been employed. Applying state space averaging technique to (21) - (24) and rewriting them in s-domain, the transfer function relating the inductor currents and the capacitor voltages to that of the switching duty cycle, d are obtained for PHC as follows:

$$\frac{i_{L1}(s)}{d(s)} = \frac{C_{o1}V_{pv1}s}{L_1C_{o1}s^2 + R_{L1}C_{o1}s + 1} \quad (25)$$

$$\frac{v_{co1}(s)}{d(s)} = \frac{V_{pv1}}{L_1C_{o1}s^2 + R_{L1}C_{o1}s + 1} \quad (26)$$

$$\frac{i_{L2}(s)}{d(s)} = \frac{C_{o2}V_{pv2}s}{L_2C_{o2}s^2 + R_{L2}C_{o2}s + 1} \quad (27)$$

$$\frac{v_{co2}(s)}{d(s)} = \frac{V_{pv2}}{L_2C_{o2}s^2 + R_{L2}C_{o2}s + 1} \quad (28)$$

The transfer functions for NHC can be obtained by interchanging V_{pv1} and V_{pv2} in the above equations.

From (25) - (28) it can be inferred that decoupled control for the inductor currents and the capacitor voltages is possible.

IV. Control Configuration of the Proposed Scheme

The control strategy for the proposed inverter is shown in Fig. 5. Gating pulses for the switching devices are generated i) to operate both the subarrays at their respective MPP, and ii) to ensure the flow of sinusoidal grid current in phase with the grid voltage. Two MPP tracking (MPPT) algorithms are used to generate two separate reference voltages, V_{mpp1} and V_{mpp2} for the two subarrays. These reference voltages, V_{mpp1} and V_{mpp2} are compared with the sensed subarray voltages, V_{pv1} and V_{pv2}, and the errors so generated are processed through two separate proportional integral (PI) controllers to generate the amplitudes of the reference currents, i_{ref1} and i_{ref2} for the inductors, L_1 and L_2. A unity sinusoidal function, X synchronized to v_g is generated by employing a phase locked loop (PLL). The signal, X is then multiplied with the generated amplitudes to obtain the reference currents i_{ref1} and i_{ref2} for controlling the inductor currents, i_{L1} and i_{L2}. During PHC, i_{ref1} and i_{ref2} are assigned to i_{L1ref} and i_{L2ref} respectively while during NHC i_{ref1}, and i_{ref2} are assigned to i_{L2ref} and i_{L1ref} respectively. i_{L1ref} and i_{L2ref} are the current references for L_1 and L_2 respectively. The sensed inductor currents i_{L1}, i_{L2} are compared with the corresponding references, i_{L1ref}, i_{L2ref} and the errors so generated are processed through two separate PI controllers to synthesize sinusoidal duty ratio profile for S_1-S_4.

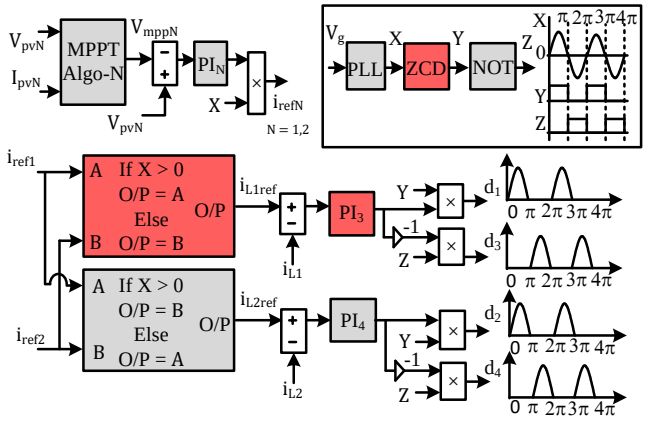

Fig. 5. Control configuration of the proposed inverter

Though output of both inverters are in series, during conditions when different magnitudes of power are being generated from the two subarrays, I_{co1} and I_{co2} differ in magnitude. This phenomenon is shown in the phasor diagram of Fig. 6 wherein the operation of the proposed inverter during PHC is depicted while considering power obtained from PV_1 being greater than that of PV_2. The phases of I_{L1} and I_{L2} with respect to V_g are ϕ_1 and ϕ_2 respectively. The voltage drops across L_1, L_2 are V_{L1}, V_{L2} and V_{HB1}, V_{HB2} are the fundamental components of output voltages of $HBIAB_1$ and $HBIAB_2$. It can be inferred from this diagram that the variation in magnitude of I_{co1}, I_{co2}, leads to a variation in phase and magnitude for the currents, I_{L1} and I_{L2} as well. Although this variation is marginal, i_{L1} and i_{L2} need to be controlled separately to stabilize the close loop operation of the proposed inverter.

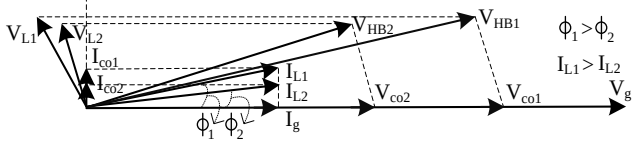

Fig. 6. Phasor diagram showing the interaction of the proposed inverter with the grid

The output variable of the plant is the injected grid current, $i_g \approx i_{L1} \approx i_{L2}$. The variable, i_{L1} is the output of the converter segment, $HBIAB_1$ while the variable, i_{L2} is the output of the converter segment, $HBIAB_2$. The relationship of i_{L1} and i_{L2} versus the duty ratio of the respective converter segments in s-domain have been derived as (25) and (27). The compensated frequency response plots of $i_{L1}(s)$ versus $d(s)$ for different values of proportional gain K_p, keeping integral gain K_i = 100 is presented in Fig. 7. The nature of the compensated frequency response plot of $i_{L2}(s)$ versus $d(s)$ is

more or less similar to that of $i_{L1}(s)$ versus $d(s)$. Therefore the frequency domain analysis of the plant is carried out based on the frequency response plot of $i_{L1}(s)$ versus $d(s)$. From Fig. 7 it can be inferred that with the decrease in the value of K_p, phase margin of the compensated system decreases, which leads to instability. If the value of K_p is increased, the phase margin increases marginally, however if K_p becomes more than 0.5, total harmonic distortion (THD) of i_g increases beyond the specified limit [30]. Hence to achieve a phase margin of 90° for the compensated system and to maintain the THD of the grid current within the specified limit, the controller parameters, K_p and K_i are selected to be 0.5 and 100 respectively.

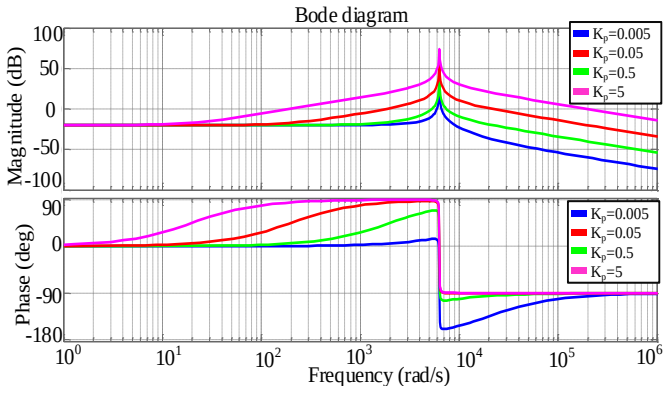

Fig. 7. Compensated bode plot of $i_{L1}(s)$ versus $d(s)$ for different values of K_p

V. Selection Criteria of Passive Elements

The passive elements used in the proposed circuit are selected based on the design procedure given in [2].

A. Selection of C_{f1} & C_{f2}

Values of C_{f1} and C_{f2} are selected based on the expression given in [2]

$$C_{f1} = C_{f2} = \frac{P_{mpp1}}{2\omega\Delta V_{ripple}V_{min}^2} = \frac{P_{mpp2}}{2\omega\Delta V_{ripple}V_{min}^2} \quad (29)$$

wherein minimum input voltage, V_{min} = 190 V, percentage of ripple in input voltage, ΔV_{ripple} = 1% of V_{min} and ω = angular grid frequency.

B. Selection of L_1 & L_2

Values of L_1 and L_2 are obtained utilizing the following expression [2]

$$L_1 = L_2 = \frac{V_{com}\Delta I_{factor}}{f_{sw}\Delta I_L} \quad (30)$$

wherein V_{com} = 190 V and maximum ripple instant factor, ΔI_{factor} = 0.12, which is selected from the characteristic of ripple factor given in [2] for modulation index = 0.87. The switching frequency, f_{sw} = 20 KHz, and the inductor current ripple, ΔI_L = 0.25 A.

TABLE I
Parameters/Elements Employed to Simulate the Proposed Inverter

Parameter	Value
Grid voltage (V_g)	230 V, 50 Hz
V_{oc}[a] & V_{mpp} of subarrays at STC[b]	270 V & 217 V
I_{sc}[c] & I_{mpp} of subarrays at STC	3.58 A & 3.22 A
P_{mpp1} & P_{mpp2} at STC	780 W
Power rating of the simulated system	1.5 KW Approx
Output filter inductors (L_1 and L_2)	5 mH
Output filter capacitors (C_{o1} and C_{o2})	5 μF
Input DC capacitors (C_{f1} and C_{f2})	3300 μF
Employed MPPT Algorithm	Incremental Conductance
Switching frequency of (S_1-S_4)	20 kHz
Switching frequency of (S_5-S_8)	50 Hz

[a] V_{oc} = Open circuit voltage of subarrays.
[b] STC = Standard test condition: Insol. = 1 KW/m^2, Temp. = 25 °C.
[c] I_{sc} = Short circuit current of subarrays.

TABLE II
Variations Imposed on Temperature & Insolation of the Subarrays for Performing Simulation Study

Time in Second	0-1	1-2	2-3	3-4	4-6	6-8
Insol. in PV_1, kW/m^2	0.7	0.8	0.9	1.0	1.0	1.0
Insol. in PV_2, kW/m^2	0.9	0.9	0.9	0.9	0.9	0.9
Temp. in PV_1 (°C)	25	25	25	25	30	35
Temp. in PV_2 (°C)	25	25	25	25	25	25

C. Selection criteria of C_{o1} & C_{o2}

C_{o1} and C_{o2} are obtained from [2]

$$C_{o1} = C_{o2} = \frac{1}{4\pi^2 f_c^2 (L_1 or L_2)} \quad (31)$$

wherein cut off frequency, f_c = 1 KHz.

VI. Simulated Performance

To verify the effectiveness of the proposed scheme while there exists a significant difference in atmospheric conditions between the two subarrays, detailed simulation studies are carried out on Matlab-Simulink platform utilizing the system parameters given in Table I. The difference in time dependent atmospheric conditions that are considered to simulate the system are given in Table II. The variation in P_{mpp1}, V_{mpp1}, I_{mpp1} of PV_1 and P_{mpp2}, V_{mpp2}, I_{mpp2} of PV_2 are shown in Fig. 8(a), 8(b), 8(c). While considering the performance of the panels at STC and noting the atmospheric conditions imposed as per Table II, it can be inferred from Fig. 8 that the proposed inverter is able to operate both the subarrays at their respective MPP.

Fig. 9 shows the response of i_g along with v_g for the entire range of operation. Its response for two and half cycles for the two different environmental conditions are also depicted. It can be inferred from these figures that the current injected to the grid remains to be sinusoidal, and in phase with the grid

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voltage even though there is a variation in power evacuated from the two subarrays.

In Fig. 10 variation in v_{co1} and v_{co2} are shown for the entire range of operation. Their responses for two and half cycles for the two different environmental conditions are also shown. It can be verified from Fig. 10 that for the condition as given in Tables I and II, the variations in V_{co1m} and V_{co2m} are as predicted by (13), (14), (15) and (16).

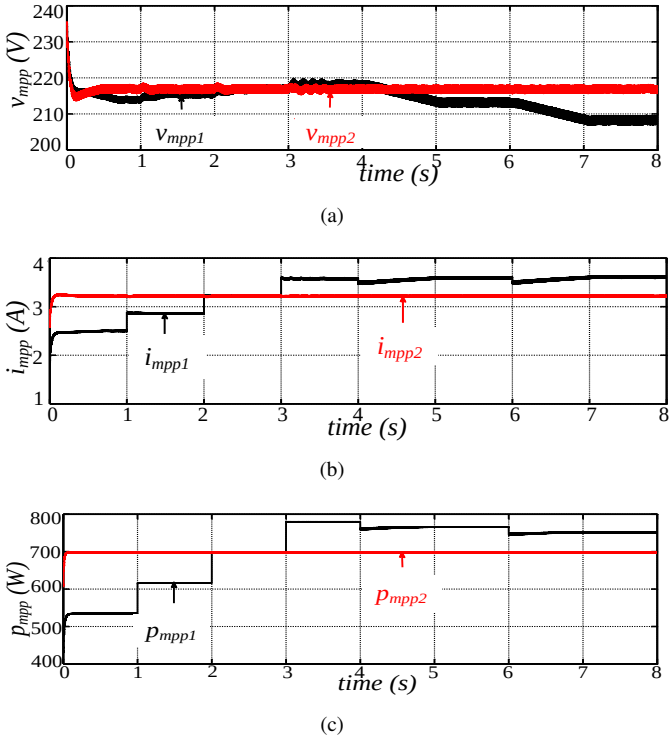


Fig. 8. Simulated performance: (a) Power output from PV_1 and PV_2, (b) Voltage output of PV_1 and PV_2, (c) Output current of PV_1 and PV_2

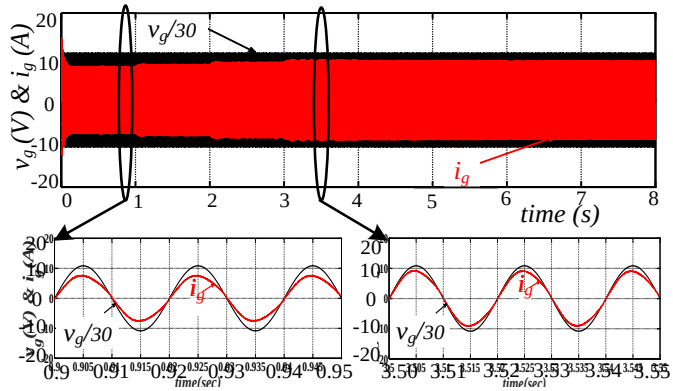


Fig. 9. Simulated performance: Grid current and voltage along with their magnified versions

VII. Experimental Validation

In order to demonstrate the viability of the proposed scheme, detailed experimental studies are carried out utilizing

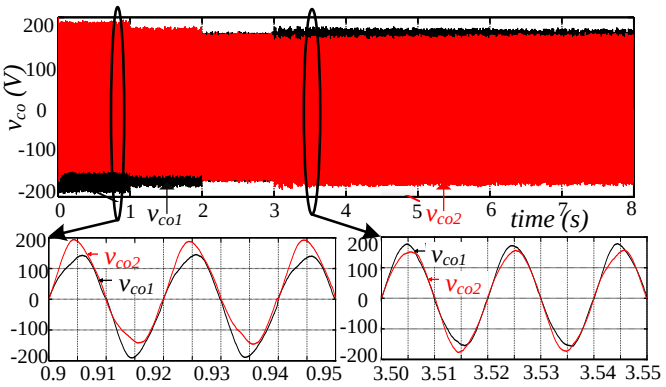


Fig. 10. Simulated performance: Output capacitor voltages along with their magnified versions

TABLE III
Parameters/Elements Employed for the Laboratory Prototype of Proposed Inverter

Parameter	Value
Grid voltage (V_g)	230 V, 50 Hz
Set V_{oc} & V_{mpp1}, V_{mpp2} in Solar Emulators at STC	1) 250 V & 200 V, 200 V 2) 250 V & 190 V, 200 V
Set I_{sc} & I_{mpp} in Solar Emulator at STC	2.922 A & 2.63 A
Power rating of the laboratory prototype	1 KW
Output filter inductors (L_1 and L_2)	5 mH, 0.2 Ω
Output filter capacitors (C_{o1} and C_{o2})	5 μF
Input DC capacitors (C_{f1} and C_{f2})	3300 μF
PV parasitic capacitors (C_{pv1} and C_{pv2})	0.1 μF
MPPT Algorithm	Incremental Conductance
SIC based Mosfets (S_1-S_4)	C2M0160120D
IGBTs (S_5-S_8)	STGF10NC60HD
Switching frequency of (S_1-S_4)	20 kHz
Switching frequency of (S_5-S_8)	50 Hz
Digital Signal Controller	TMS320F28335

a 1 kW laboratory prototype of the scheme fabricated for the purpose.

The pertinent parameters related to the prototype are given in Table III. Switching devices are selected based on loss calculation provided in [11]. Two programmable EPS PSI9360-15 power supplies with solar PV emulation feature are employed to realize PV_1 and PV_2. The photograph of the overall experimental setup is shown in Fig. 11

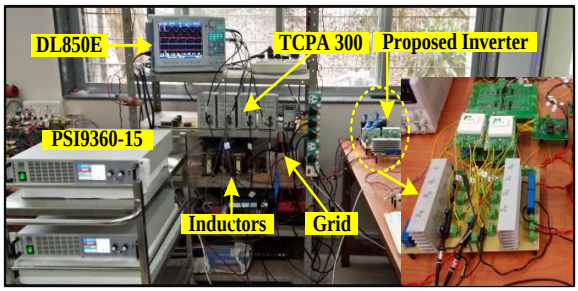


Fig. 11. Photograph of the experimental setup

TABLE IV
EXPECTED VARIATION IN I_{mpp}, P_{mpp}, V_{com} DURING PV_1 INSOLATION VARIATION WHEN V_{mpp1} = 200 V, V_{mpp2} = 200 V

% Insol. of PV_1	100	90	80	70
% Insol. of PV_2	90	90	90	90
I_{mpp1} (A)	2.63	2.367	2.104	1.841
I_{mpp2} (A)	2.367	2.367	2.367	2.367
P_{mpp1} (W)	526	473.4	420.8	368.2
P_{mpp2} (W)	473.4	473.4	473.4	473.4
V_{co1m} in PHC or V_{co2m} in NHC (V)	171.2	162.63	153	142.3
V_{co2m} in PHC or V_{co1m} in NHC (V)	154	162.63	172.2	183

To demonstrate the effectiveness of the proposed inverter in realizing MPP operation of the two PV subarrays, PV_1 and PV_2 while there exists significant difference in insolation level between them, the parameters, V_{oc}, V_{mpp}, I_{mpp} of both the PV subarrays are set as mentioned in Table III. The insolation of PV_2 is kept constant, while that of PV_1 is varied in the manner as shown in Table IV. The estimated values of I_{mpp}, P_{mpp}, V_{com} during the entire range of aforementioned insolation variation are also indicated in the same table. The measured variations in P_{mpp}, I_{mpp}, i_g are shown in Fig. 12. Zoomed version of the responses over four cycles for the two different environmental conditions are shown in Fig. 13(a), 13(b). Measured values of I_{mpp}, P_{mpp}, V_{com}, I_{gm} as indicated in Fig. 13(a), 13(b) are more or less same as that of estimated values provided in Table IV thereby validating the capability of the proposed inverter to extract maximum power from two subarrays during mismatched insolation condition.

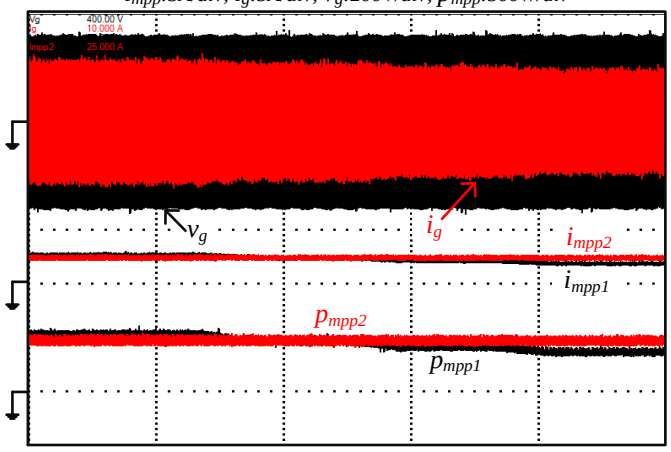
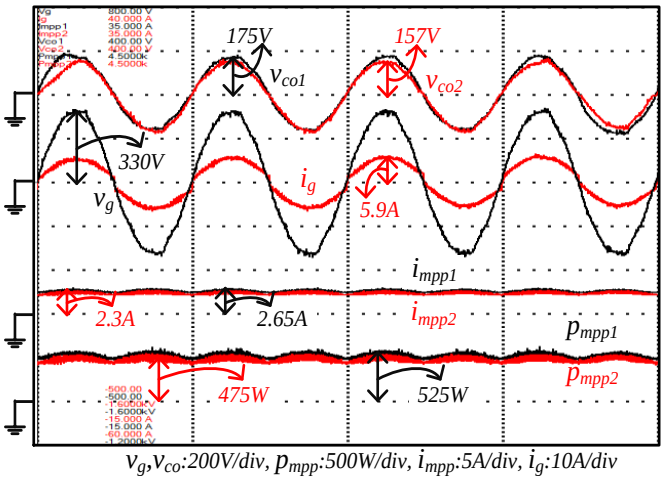
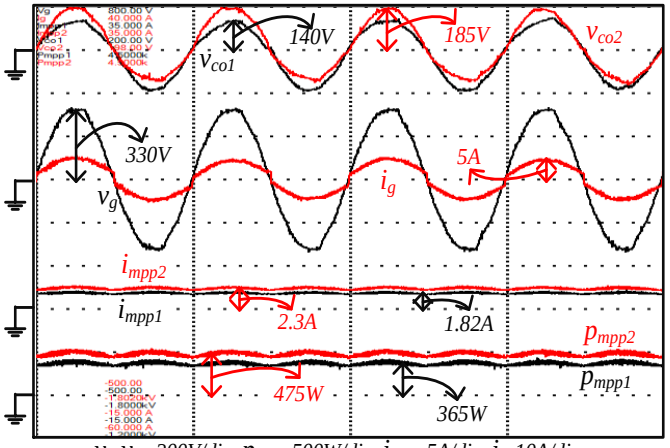


Fig. 12. Experimental performance: v_g, i_g, P_{mpp}, I_{mpp} throughout the operating range under varied insolation level

The programmable power supply EPS PSI9306-15 available in the laboratory has provision to vary only the insolation level while there is no feature to change the setting for temperature. In order to emulate temperature variation, V_{mpp1} is set at 190 V and V_{mpp2} is set at 200 V as variation in temperature changes V_{mpp} significantly while I_{mpp} experiences insignificant change. Difference in voltages is selected to be 10 V to replicate a temperature difference of around $10°C$ as per the data sheet of solar module from 'BP solar' [32]. Rest of



(a)



(b)

Fig. 13. Experimental performance: Magnified view of v_{co}, v_g, v_g, I_{mpp}, P_{mpp} when (a) PV_1 insolation=100% & PV_2 insolation=90%, (b) PV_1 insolation=70% & PV_2 insolation=90%

TABLE V
EXPECTED VARIATION IN I_{mpp}, P_{mpp}, V_{com} DURING PV_1 INSOLATION VARIATION WHEN V_{mpp1} = 190 V, V_{mpp2} = 200 V

% Insol. of PV_1	100	90	80	70
% Insol. of PV_2	90	90	90	90
I_{mpp1} (A)	2.63	2.367	2.104	1.841
I_{mpp2} (A)	2.367	2.367	2.367	2.367
P_{mpp1} (W)	500	450	400	350
P_{mpp2} (W)	473.4	473.4	473.4	473.4
V_{co1m} in PHC or V_{co2m} in NHC (V)	167	158.5	149	138.3
V_{co2m} in PHC or V_{co1m} in NHC (V)	158.2	167	176.3	187

the settings and variation in insolation are kept similar to that of the previous case and are given in Table III and V. The estimated values of I_{mpp}, P_{mpp}, V_{com} for the entire operating range are also indicated in Table V. Fig. 14 shows the variation of i_g, I_{mpp}, P_{mpp}, v_{co} for the specified range of insolation variation as mentioned in Table V. Zoomed version of their responses for four cycles for the two different environmental conditions are also shown in Fig. 15(a) and 15(b). Measured

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values of V_{mpp}, I_{mpp}, P_{mpp}, V_{com}, I_{gm} as indicated in Fig. 15(a) and 15(b) are more or less same as that of estimated values provided in Table V thereby validating the capability of the proposed inverter to extract maximum power from two PV subarrays during any mismatched environmental condition.

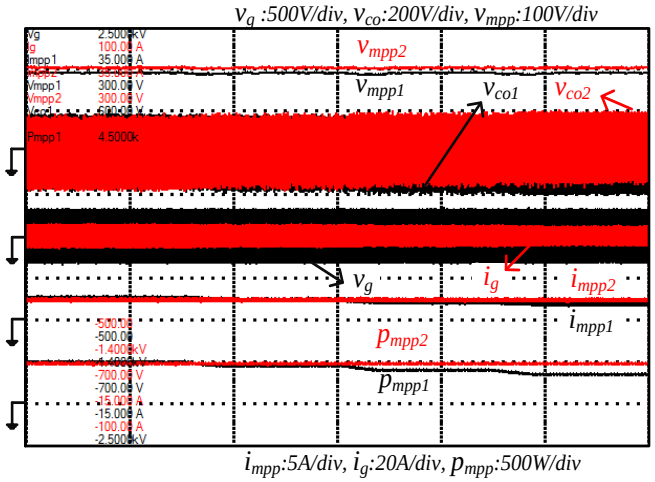

Fig. 14. Experimental performance: v_{co}, i_L, V_{mpp}, I_{mpp}, P_{mpp} throughout the operating range under varying insolation level and module temperature

The response of i_g along with v_g for insolation variation and emulated temperature variation are also shown in Fig. 13 and Fig. 15 respectively. It can be inferred from these figures that the current injected to the grid remains to be sinusoidal, and in phase with the grid voltage even though there is a variation in power evacuated from the two subarrays.

Fig. 16 shows Fast Fourier Transform (FFT) of the grid current i_g. THD of i_g is determined following the procedure specified in the standard, IEEE 1574/IEC 61727 [30], [29] and is found to be 4.35% which is below 5% which is the limit specified in the aforementioned standard.

To measure the leakage current flowing through the PV parasitic capacitors (C_{pv0}, C_{pv1}, C_{pv2}), 0.1 μF polypropylene film capacitors are connected to emulate the role of C_{pv1}, C_{pv2}. Fig. 17 shows the voltage, v_{cpv1} impressed across C_{pv1} and the voltage, v_{cpv2} impressed across C_{pv2} along with the leakage current, i_{cpv2} flowing through C_{pv2}. Rms value of i_{cpv2} is found to be 9.80 mA which is much lower than 30 mA, the limit being specified in German standard code VDE 0126-1-1 [29], [31]. Although 0.1 μF capacitor is considered to emulate the PV parasitic capacitor, according to the procedure for selecting the value of parasitic capacitor as given in [31] much lower value for the emulated PV parasitic capacitor can be chosen for the proposed scheme as in this case the power negotiated by each PV subarray is half of the total power. Thus the actual leakage current in the proposed scheme is much smaller than 9.80 mA.

Fig. 18 shows the estimated and measured efficiency curve of the proposed inverter. The Yokogawa make power analyzer, WT1800 is used to measure the efficiency. The efficiency is measured considering the losses incurred in all the power devices and filter elements while excluding the losses associated with the control circuit. The measured peak efficiency is found to be 97% and the measured European efficiency (η_{euro}) is found to be 96%. For the topologies dealing with unbalanced generating conditions, the reported η_{euro} in [28] is 91.22% while the highest η_{euro} ($\eta_{euro} = 95.7\%$) is reported in [20]. However, it may be noted that this efficiency of 95.7% is obtained while both the subarrays are experiencing similar atmospheric conditions. If there is a difference in environmental conditions the efficiency of the scheme of [20] falls as the extent of atmospheric difference existing between the two subarrays increases.

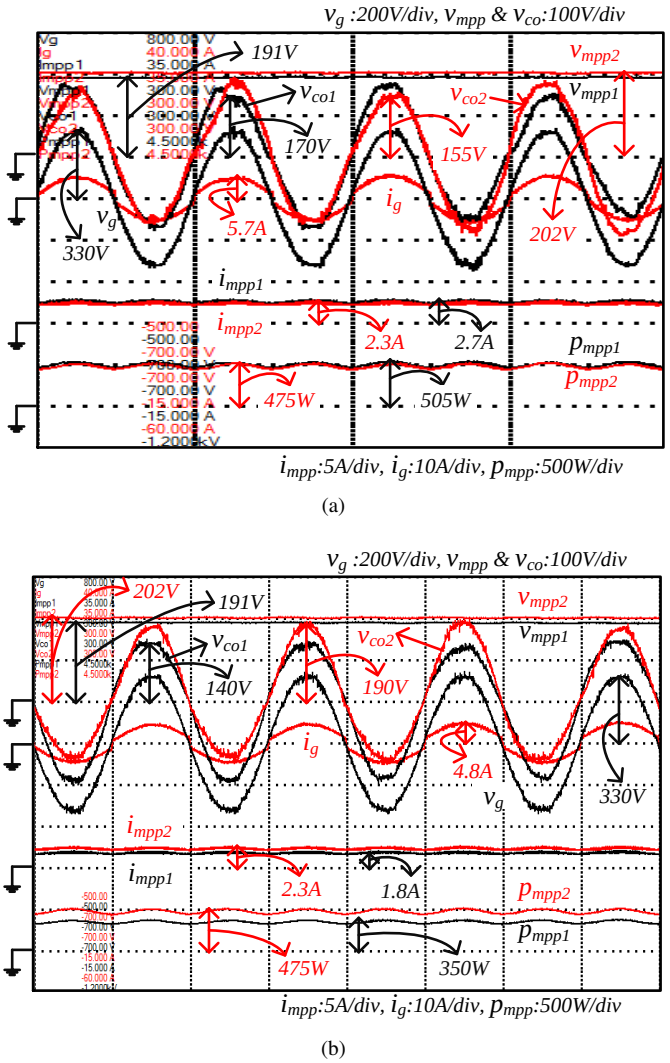

Fig. 15. Experimental performance: Magnified view of v_{co}, i_L, V_{mpp}, I_{mpp}, P_{mpp} with difference in input voltages when (a) PV_1 insolation=100% & PV_2 insolation=90%, (b) PV_1 insolation=70% & PV_2 insolation=90%

In order to verify the transient performance of the proposed scheme, the total output from the solar emulators is step changed from 325 W to 975 W at 1.35 s and at 1.45 s it is step changed from 975 W to 325 W while the grid voltage is maintained constant at 230 V. The response of the measured grid current for the aforesaid test condition is presented in Fig. 19(a) and from this figure it can be inferred that the response

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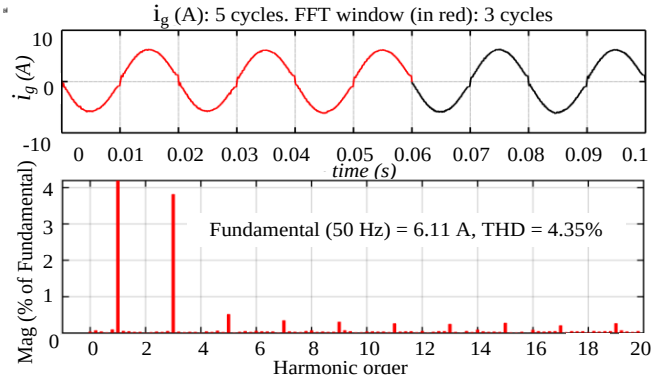

Fig. 16. Experimental performance: FFT of i_g

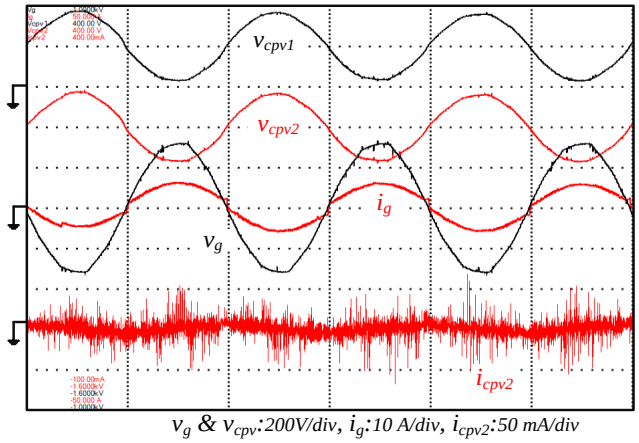

Fig. 17. Experimental performance: v_{cpv1}, v_{cpv2}, i_{cpv2}

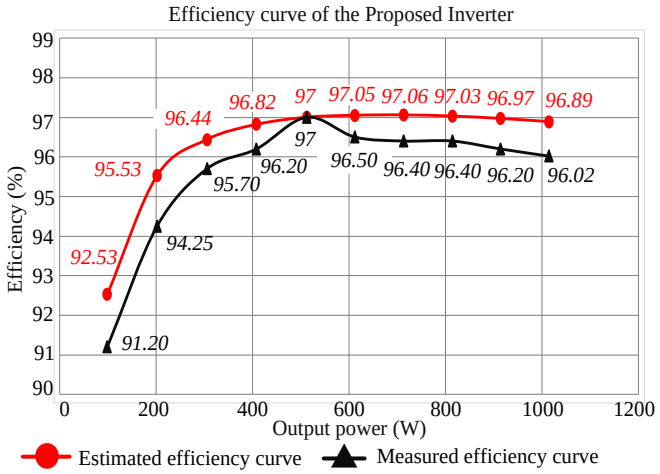

Fig. 18. Efficiency curve of the Proposed inverter

of the system is almost instantaneous without showing any oscillatory behavior. In order to demonstrate the behavior of system in the event of a disturbance in the grid voltage, a dip of 80 V is introduced on the grid voltage from 1.5 s to 2 s while the references for the current controllers are intentionally set at the rated value of the system. The response of the system during aforesaid test condition is shown in Fig. 19(b) and from this it can be inferred that the system can ride through situations arising due to disturbance in the grid voltage.

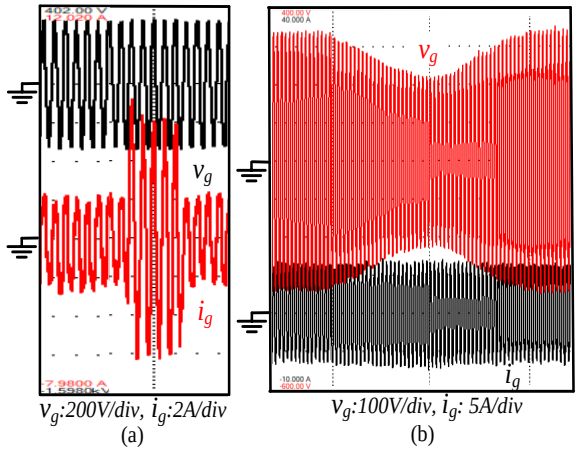

Fig. 19. Experimental performance: (a) Power reference change in sequence of 325 W - 975 W - 325 W, (b) Grid voltage dip in sequence of 230 V - 150 V - 230 V

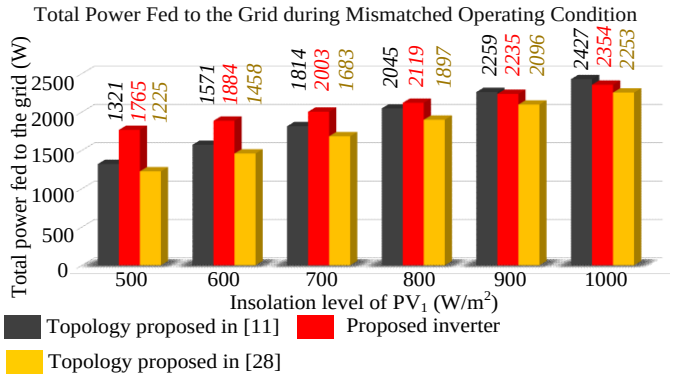

Fig. 20. Power fed to the grid by Topology [11], Topology [28] & Proposed inverter during mismatched operating condition

To evaluate the power yield of various inverters while the solar subarrays are experiencing mismatched atmospheric conditions, a 2.5 KW transformerless system at STC is simulated. The simulated PV system consists of two PV subarrays, PV_1 & PV_2 connected in series wherein 7 BP solar modules 'BP4175B' [32] are connected in series to form each of the subarray. This PV system is used to evaluate the power yield of the following inverters: (1) the proposed inverter, (2) the H-bridge based inverter presented in [11] having η_{euro} of 99% (@20 KHz) which is having the highest efficiency reported in the literature and (3) the inverter presented in [28] having η_{euro} of 91.22% which is also having the capability of servicing two separate PV subarrays under mismatched atmospheric condition. Insolation level of PV_2 is maintained at 100% i.e. at STC while that of PV_1 is varied in steps of 10% from 100% to 50%. While estimating the power yield from the subarrays, it is assumed that the employed MPPT algorithm is able to track

the global MPP of the subarrays. The total power extracted from the two subarrays is then multiplied by the reported or estimated η_{euro} of the respective schemes to get the estimated power yield from each of them. The estimated power yields for the aforementioned conditions from the proposed scheme, the scheme reported in [11] and that of [28] are depicted in Fig. 20. It can be inferred from Fig. 20 that the proposed scheme is most effective in abstracting power from the solar PVs under mismatched operating conditions.

VIII. Conclusion

A grid connected single phase transformerless inverter which can extract maximum power from two subarrays during mismatched operating condition is presented in this paper. Salient features of the proposed inverter are as follows: i) number of series connected modules is less thereby reducing the effect of shading, ii) two subarrays can be operated at MPP simultaneously, thus it is well suited for PV subarrays operating under mismatched operating condition, iii) decoupled control structure is employed to control the two component half bridges of the inverter, iv) η_{euro} of 96% is achieved which is the highest compared to the topologies dealing with solar PVs experiencing mismatched operating conditions, v) the scheme is realized through single stage of power conversion leading to a considerable reduction in size, weight and volume, vi) simple MPPT algorithm is employed thereby reducing the computational burden of the digital signal processor involved, vii) PV leakage current is limited within the limit specified in the standard, VDE 0126-1-1. The operating principle of the proposed scheme is explained in detail by exploring all the equivalent topological stages. Subsequently the mathematical analysis of the scheme has been carried out and the small signal model of the scheme has been derived. The philosophy of control is described in detail and the configuration of the controller is derived. The design guidelines for selecting the filter components of the inverter are presented. Detailed simulation and experimental studies are carried out to confirm the viability of the proposed scheme.

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